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**module ripple\_counter(q, clk, reset);**

**output [3:0] q;**

**input clk, reset;**

**T\_FF tff0 (q[0], clk, reset);**

**T\_FF tff1 (q[1], q[0], reset);**

**T\_FF tff2 (q[2], q[1], reset);**

**T\_FF tff3 (q[3], q[2], reset);**

**endmodule**

**module T\_FF (q, clk, reset);**

**output q;**

**input clk, reset;**

**wire d;**

**D\_FF d0 (q, d, clk, reset);**

**not n1 (d, q);**

**// not is a Verilog-provided primitive. Case sensitive.**

**endmodule**

**module D\_FF (q, d, clk, reset);**

**output q;**

**input d, clk, reset;**

**reg q;**

**always @(posedge reset or negedge clk)**

**begin**

**if (reset)**

**q = 1'b0;**

**else**

**q = d;**

**end**

**endmodule**

**module stimulus;**

**reg clk;**

**reg reset;**

**wire[3:0] q;**

**ripple\_counter rc (q, clk, reset);**

**always**

**#5 clk = ~clk; //toggle clk every 5 time units**

**initial**

**begin**

**clk = 1'b0; //set clk to 0**

**reset = 1'b1;**

**#15 reset = 1'b0;**

**#500 $finish; //terminate the simulation**

**end**

**// monitor the outputs**

**initial**

**$monitor($time, " Output q = %d", q);**

**endmodule**